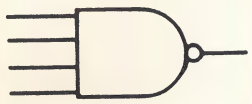
91-050
May 1965
New information

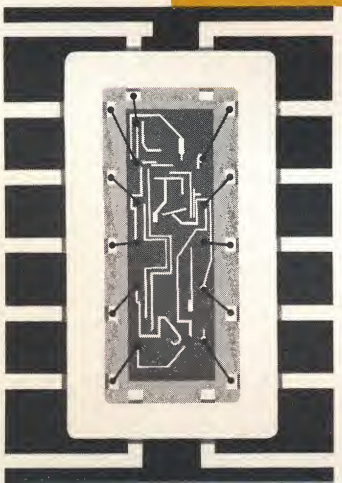


QUICK REFERENCE GUIDE

Molecular Electronics Division

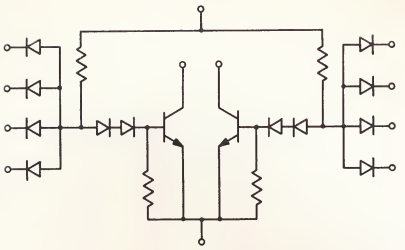
INTEGRATED CIRCUITS

COMMERCIAL DTL LINE

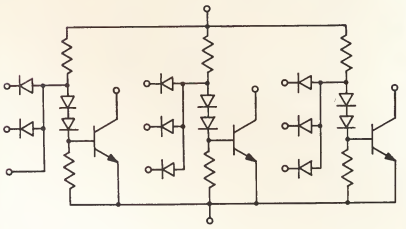


industrial-commercial integrated circuits

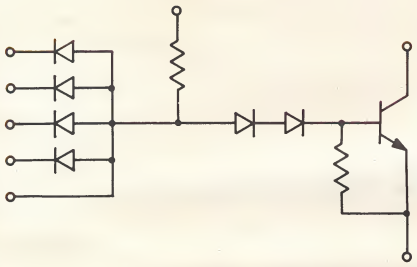
WC 211 G,T Dual NAND Gate
4 input



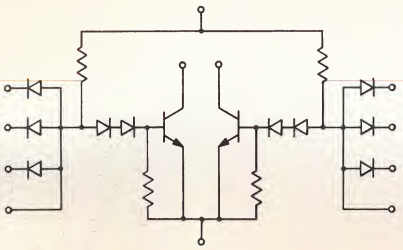
WC 206 G Triple NAND Gate
Two 3 inputs; one 2 input with node



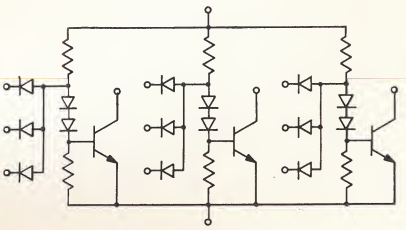
WC 204 G,T Single NAND Gate
4 input with node



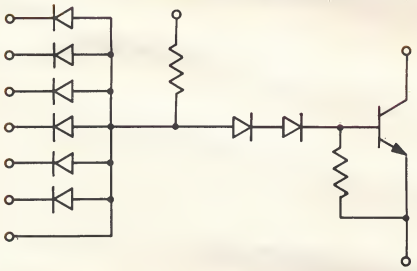
WC 221 G,T Dual NAND Gate
3 input with nodes



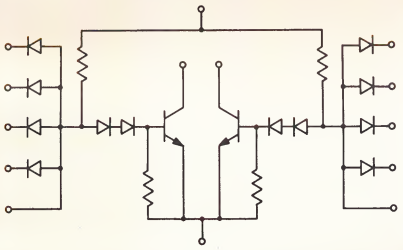
WC 216 G Triple NAND Gate
Three 3 inputs



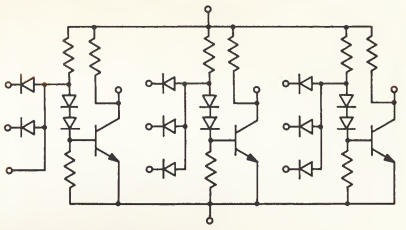
WC 214 G,T Single NAND Gate
6 input with node



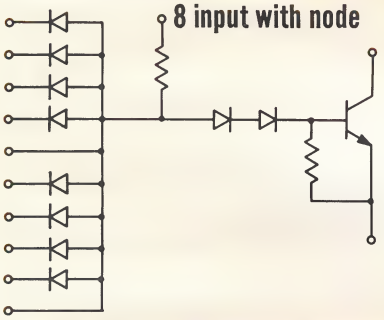
WC 231 G Dual NAND Gate
4 input with nodes



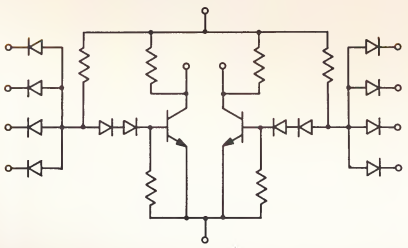
WC 226 G Triple NAND Gate
Two 3 inputs, one 2 input
with node, collector resistors



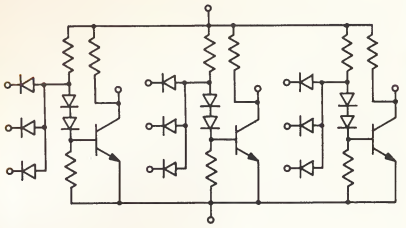
WC 224 G,T Single NAND Gate
8 input with node



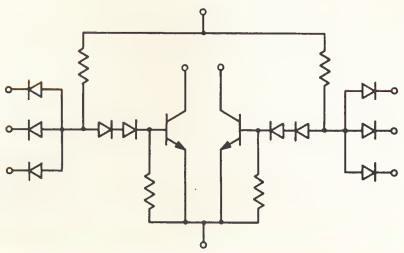
WC 241 G Dual NAND Gate
4 input with collector resistors



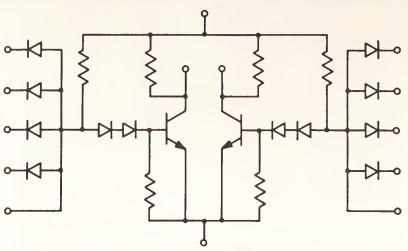
WC 236 G Triple NAND Gate
Three 3 inputs, collector resistors



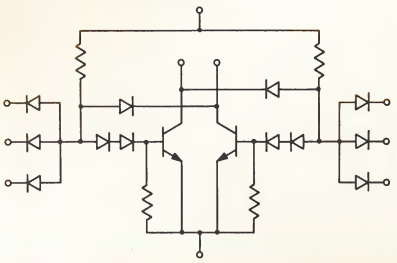
WC 201 G,T Dual NAND Gate
3 input



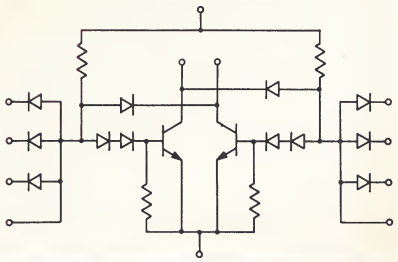
WC 261 G Dual NAND Gate
4 input with nodes, collector resistors



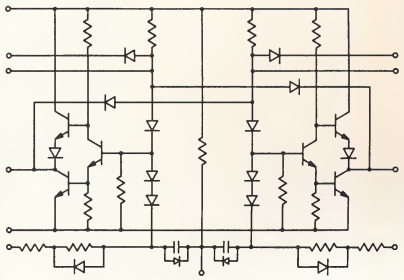
WC 202 G,T
RS flip flop 3 input



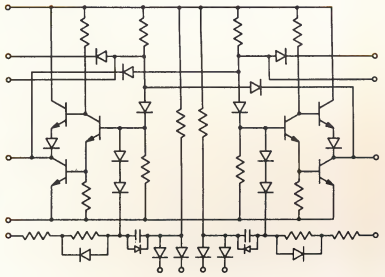
WC 212 G,T RS flip flop
3 input with nodes



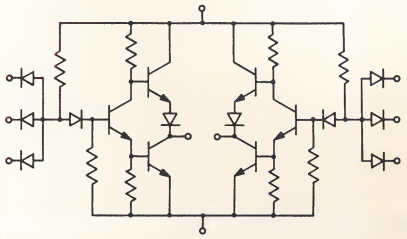
WC 213 G,T pulse binary counter



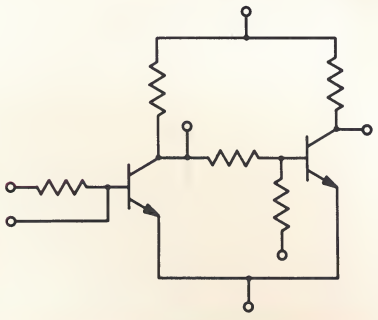
WC 215 G,T JK flip flop



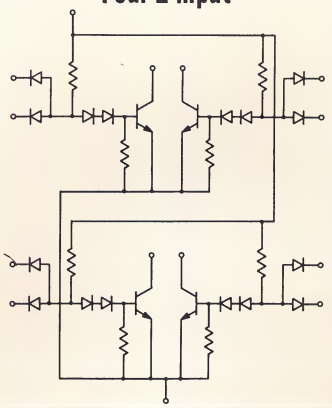
WC 210 G,T line driver
Two 3 input



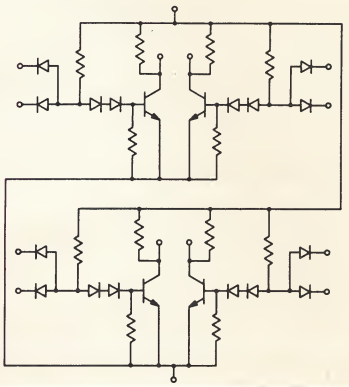
WC 208 G,T Level Detector-Schmitt Trigger



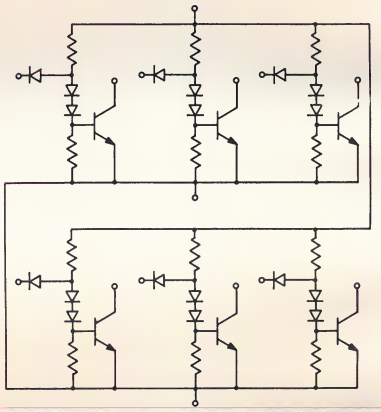
WC 246 G Quad NAND Gate
Four 2 input



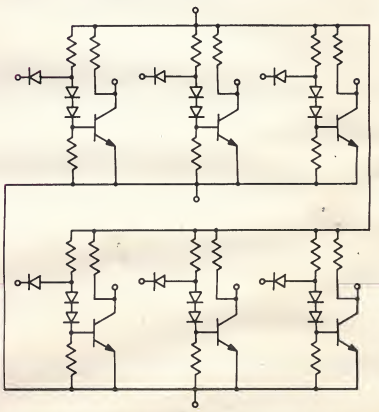
WC 266 G Quad NAND Gate
Four 2 input; collector resistors



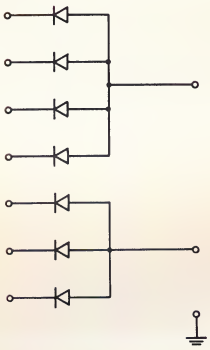
WC 286 G Hex NAND Gate
Six 1 input



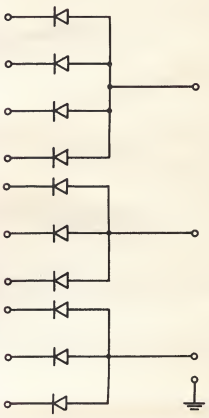
WC 296 G Hex NAND Gate
Six 1 input; collector resistors



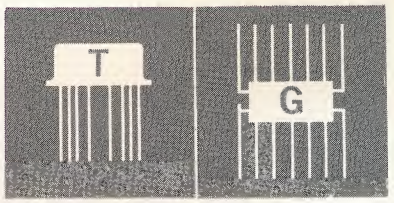
WC 217 G,T
diode array



WC 227 G,T diode array



packages



8 or 12 lead TO-5 pack

14 lead ¼" x ⅛" FLAT-PAK™

Electrical Characteristics

parameter	symbol	limit	values at temperature +25°C	values at temperature 0° to 75°C worst case	units
STANDARD GATE CHARACTERISTICS (FOR V_{cc}=6.0 VOLTS)					
power consumption, per gate, 50% duty cycle	P_c	max. typ.	9.5 7.5	10.5	mw mw
input current, input grounded	I_{in}	max.	1.80	2.10	ma
input voltage for 0-state output, fan-out of six	$V_{in}/0$	min.	1.80	2.10	volts
input voltage for 1-state output, fan-out of one	$V_{in}/1$	max.	1.00	0.60	volts
output current @ specified $V_{CE(SAT)}$	I_{out} $V_{CE(SAT)}$	min. typ. max.	20 32 0.45		ma ma volts
fan-out available each gate	F_o	min.	11	6	...
noise margin, worst case	$\triangle V_n$	typ. min.	1.00 0.55	0.25	volts
average switching time $(T_{on} + T_{off}) \div 2$	T_{avs}	typ. max.	23 32	23	ns
ring propagation delay time, (ring of five gates)	T_{rpd}	typ.	30	30	ns
SPECIAL CHARACTERISTICS (FOR V_{cc}=6.0 VOLTS)					
WC 213 power consumption, total	P_c	max. typ.	50 35	52 39	mw mw
fan-out available each output @ standard $V_{CE(SAT)}$	F_o	min.	9	7	...
count rate	f_c	min. typ.	10 12	8 10	mc mc
WC 215 power consumption, total	P_c	max. typ.	56 45	65 52	mw mw
fan-out available each output @ standard $V_{CE(SAT)}$	F_o	min.	9	7	...
count rate	f_c	typ.	5	4	mc
WC 210 power consumption, total, 50% duty cycle	P_c	max.	33	36	mw
input current, input grounded	I_{in}	max.	1.80	2.10	ma
output current @ $V_{CE(SAT)}$ = 0.60 volts	I_{out}	min.	40	30	ma
fan-out available each output @ standard $V_{CE(SAT)}$ and I_{in}	F_o	min.	17	12	...
average switching time $(T_{on} + T_{off}) \div 2$	T_{avs}	max. typ.	75 53	100 71	ns ns
ring propagation delay time, (ring of five drivers)	T_{rpd}	typ.	45	52	ns

All values shown subject to design change for product improvement.

Features

- Fan-out 11 minimum
- Noise margin typically greater than 1 volt—guaranteed minimum 550 mv
- 19 ns average switching time
- 9.5 mw maximum power consumption per gate
- Single 6 volt power supply required
- 0° to +75°C temperature range
- AND-OR-NOT function in one stage
- Compatible driver: fan-out 17 minimum; drives 40 ma, 250 pf
- Compatible binary counter and shift register elements; dc and ac coupled; counting rates to 12 mc
- Expandable fan-in through diode arrays
- 14 lead ¼" x ⅛" G style FLAT-PAK™ makes possible increased logic power per package

Westinghouse Electric Corporation

MOLECULAR ELECTRONICS DIVISION

Box 7377, Elkridge, Maryland 21227 ■ Box 305, Newbury Park, California 91320

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You can be sure if it's Westinghouse

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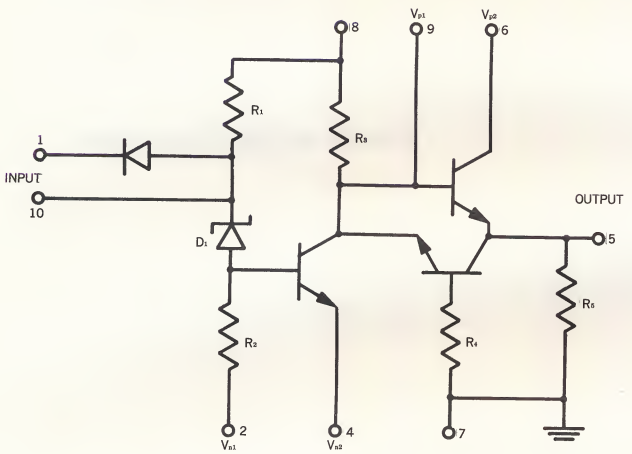
Equivalent circuit



R1 3KΩ
R2 25KΩ
R3 3.6KΩ
R4 6KΩ
R6 4KΩ
D1 9 volt Zener

Function and application

The WS 150Q is a monolithic planar epitaxial silicon integrated circuit with an input compatible with a digital device output. It converts a zero level logic input into a positive output voltage and a one level logic input into an equal negative output voltage. It is characterized by a very low output impedance for minimum output level change with loading.

The WS 150Q finds application in digital to analog conversion equipment and is compatible with other logic units of the Westinghouse WS 800 family of four volt devices.

Design features

- Low output impedance
- Precise analog output voltage
- Accepts standard 800 series logic level inputs

Reliability assurance

Mechanical and environmental reliability assurance EVERY unit receives

- High temperature storage bake at +150°C
- 3 cycles of thermal shock —55°C to +150°C
- 20,000 G centrifuge
- Gross and helium hermeticity tests

WS 150Q

interface circuit—level shifter

technical data 91-180

Absolute maximum ratings①

Parameter	Symbol	Value	Units
Supply voltage	V_{p1}	13	volts
Supply voltage	V_{p2}	10	volts
Supply voltage	V_{n1}	− 13	volts
Supply voltage	V_{n2}	− 10	volts
Input voltage	V_{in}	+ 10	volts
Output voltage	V_{out}	± 10	volts
Ambient storage temperature	T_{stg}	− 65 to + 175	°C
Ambient operating temperature	T_{opg}	− 55 to + 125	°C

Static Electrical Characteristics @ 25°C

for $V_{p1} = 10V$, $V_{p2} = 6.4V$, $V_{n1} = -10V$, $V_{n2} = -6.4V$

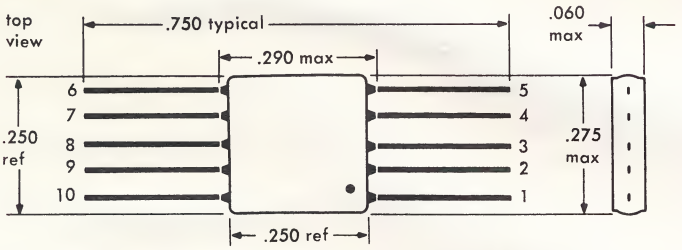
Parameter	Limit	Symbol	Value	Units
Power consumption	max.	Pc	100	mw
Input current (input grounded)	max.	In	4.5	ma
Output impedance	max.	Zo	10	ohms
Output voltage for "0" state input ②	min.	Vo, 1	+6.3	volts
Output voltage for "1" state input ②	max.	Vo, 0	−6.3	volts

Power supply application restriction

V_{p1} must be more positive than V_{p2} by at least 2.75 volts
V_{n1} must be more negative than V_{n2} by at least 0.7 volt

Package

Q style FLAT-PAK • 0.25 grams



Gold plated Kovar® leads are 15 x 5 mils on 50 mil centers. Lid and base of package are Kovar.

Pin connections

1 Input
2 − 10 volt supply, V_{n1}
3 No connection
4 − 6.4 Volt Supply, V_{n2}
5 Output
6 6.4 Volt Supply, V_{p2}
7 Ground
8 10V Supply, V_{p1}
9 Resistor measurement point
10 Diode measurement point

① Limiting values beyond which the serviceability of the device may be impaired.
② The "1" logic level is defined as 2.5 to 9.0 volts
The "0" logic level is defined as 0 to 1.5 volts

Further information

Selling policy: catalog 91-000
Prices: section 91-120

Westinghouse Electric Corporation / *MOLECULAR ELECTRONICS DIVISION*

BOX 7377 ELKRIDGE, MARYLAND 21227 • BOX 305 NEWBURY PARK, CALIFORNIA 91320

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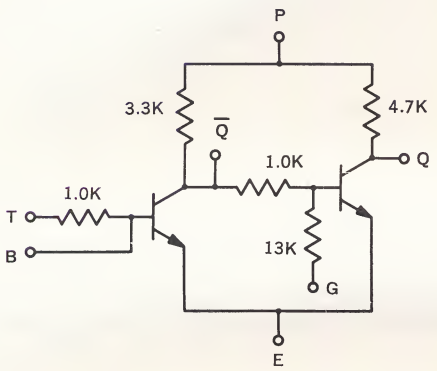
Equivalent circuit



Resistance values shown are typical

Circuit function

The level detector is designed to give an output signal determined by the voltage level at the input. The output transistor will be on (low voltage output) for voltages below the limiting value and off (high voltage output) for voltages above the limiting value. The triggering level is determined by the emitter-to-ground element used. Very low on-off hysteresis is obtainable if a zener diode is used as the level setting device between pin E and ground (pin G).

Design features

- Schmitt Trigger Operation
- Low Hysteresis
- Low Triggering Current
- Low Power Consumption
- Triggering Voltage Adjustable
- Compatible With DTL Gates

Reliability assurance

EVERY unit receives

- High temperature storage bake at +150°C
- 3 cycles of thermal shock −55°C to +150° C
- 20,000 G centrifuge
- Gross and helium hermeticity tests

Packages and type numbers		
T	G	Q
WM 208T	WM 208G	WM 208Q

Letter suffixes T, Q, and G indicate standard body style. For details on number and configuration of leads see individual package drawings.

Absolute maximum ratings①

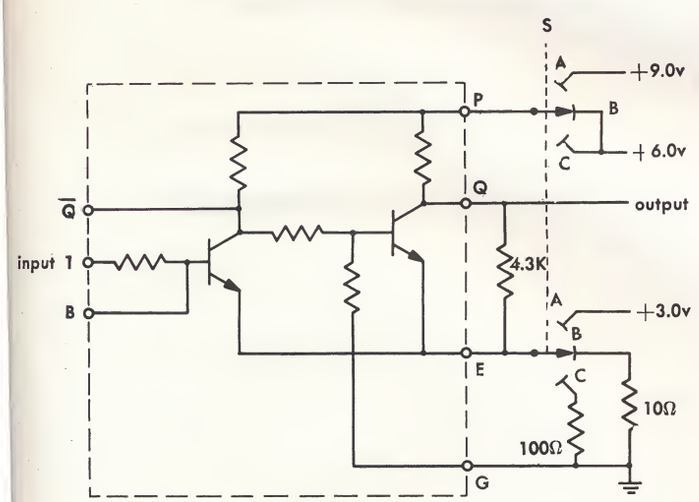
Parameter	Symbol	Valve	Units
Supply voltage	V_{PG}	+ 12	volts
Input voltage	V_{TG}	− 6	volts
Ambient storage temperature	T_{stg}	− 65 to + 175	°C
Ambient operating temperature	T_{opg}	− 55 to + 125	°C

Electrical characteristics, V_{PE} = 6.0V and R_{QE} = 4.3K

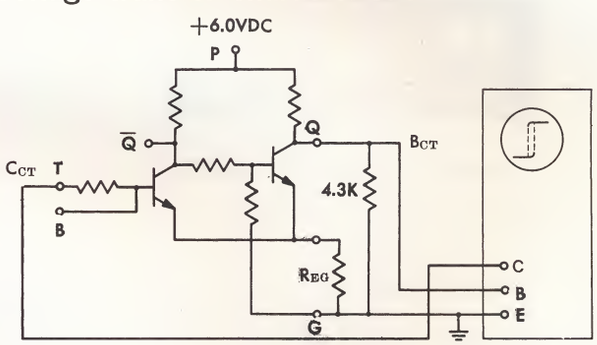
(Refer to Test Circuit)	Parameter	Min.	Typ.	Max.	Units
Input ON② (25°C to +50°C)					
Test Ckt. Condition (A) S_A	V_{TE}	.6	.8	.9	units
Test Ckt. Condition (B) S_B	V_{TG}	.6	.8	.9	volts
Test Ckt. Condition (C) S_C	V_{TG}	.9	1.0	1.2	volts
Input ON −20°C					
Test Ckt. Condition (A) S_A	V_{TE}	.6	.9	1.0	volts
Test Ckt. Condition (B) S_B	V_{TG}	.6	.9	1.0	volts
Test Ckt. Condition (C) S_C	V_{TG}	.9	1.1	1.3	volts
Input ON—OFF differential (−20°C to +50°C)				.1	volts
Input ON—OFF differential spread (−20°C to +50°C)				.4	volts
ON input current	I_T②			200	μa
ON output (−20°C to +50°C)	V_{QE}	2.5			volts
OFF output (−20°C to +50°C)	V_{QE}			.3	volts
Operating frequency (sinewave input, 1 volt peak to peak)	f_o	1			Mcps

① Limiting values beyond which serviceability of device may be impaired.
② Input OFF = Maximum increasing input voltage at which $V_{QE} \leqq$ .3 volts = Output OFF
Input ON = Minimum decreasing input voltage at which $V_{QE} \geqq$ 2.5 volts = Output ON
All values are subject to change for improvement of product.

Test circuits



Voltage transfer characteristic



Circuit for viewing voltage transfer function characteristic on a transistor curve tracer (see Figure 3).

Settings:		
	Vertical	0.5v/div (V_B)
	Horizontal	0.2v/div (V_C)
	Base Step	Open
	Collector Sweep	2 Volts

NOTE: The load resistor in the test circuit, R_{QE}, is connected between the output and the emitters for simplicity; the load resistor in the voltage transfer function circuit and for the typical characteristic curves, R_{QG}, is connected between the output and ground so that the hysteresis, V_{DIF}, is dependent upon R_{EG} only.

Typical electrical characteristics

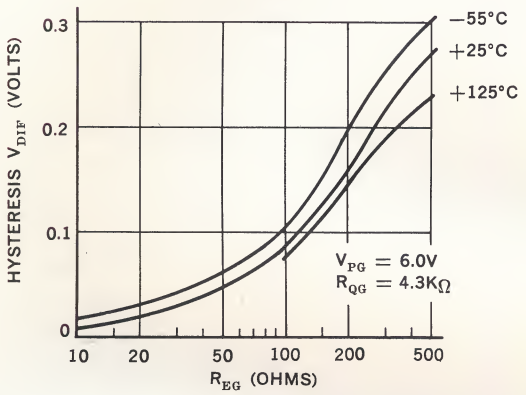


Figure 1

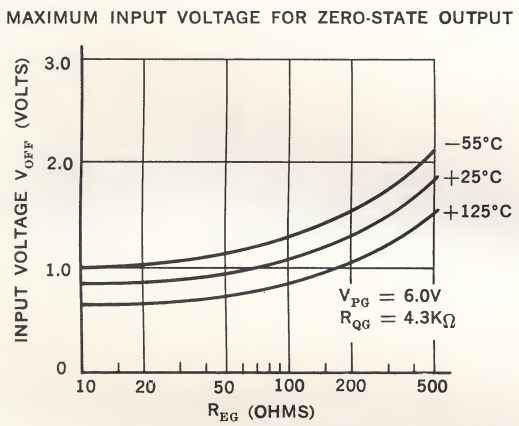


Figure 2

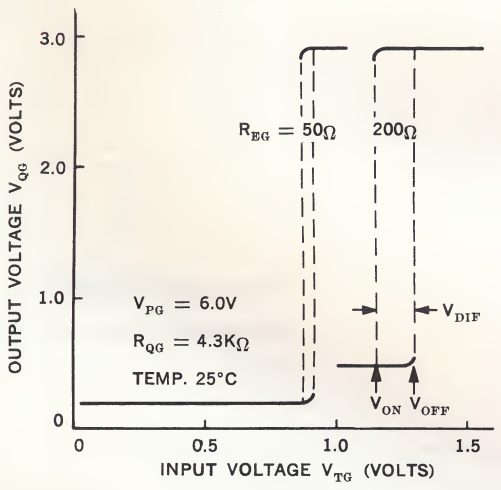


Figure 3

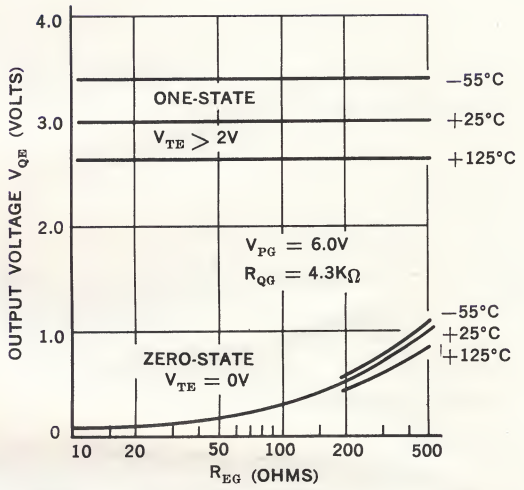


Figure 4

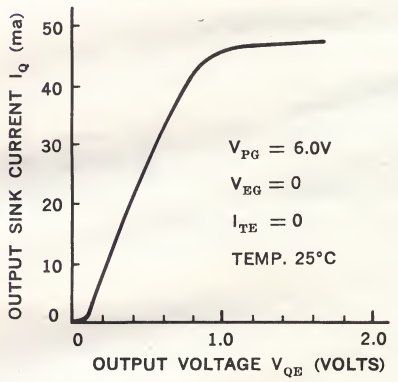


Figure 5

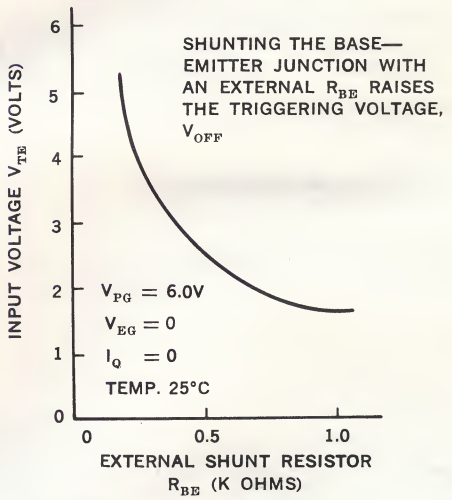


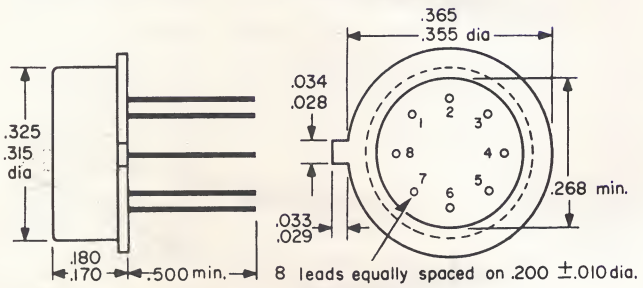
Figure 6

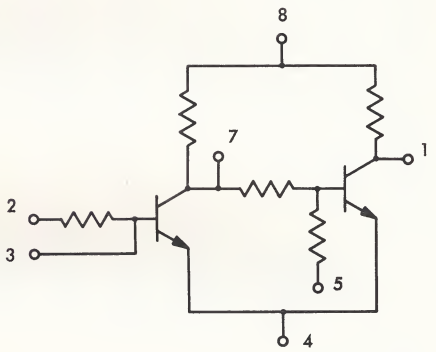
WM 208T
WM 208G
WM 208Q
(formerly WS 113)

level detector

technical data 91-197

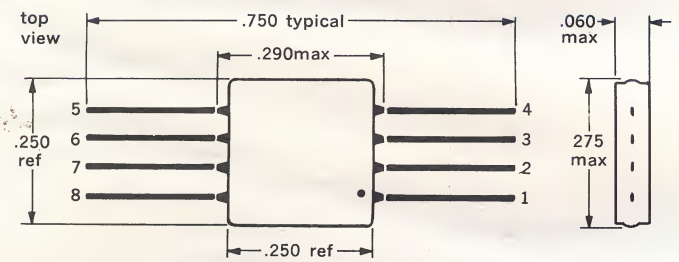
T package 8 pins • 1.05 grams

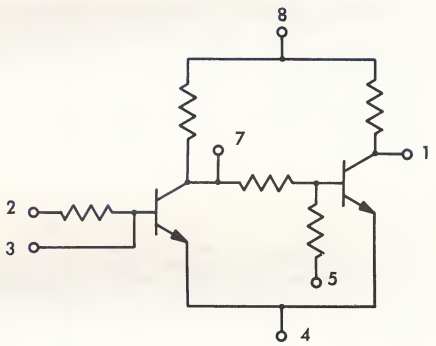




8 lead $\frac{.016}{.019}$ diameter gold plated KOVAR.

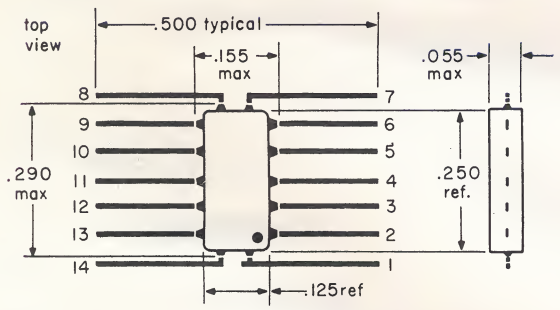
Q style FLAT-PAK® • 0.25 grams

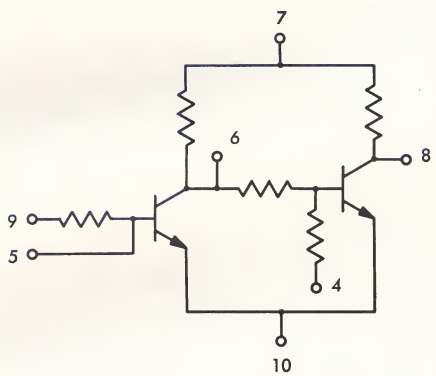




Gold plated Kovar® leads are 15 x 5 mils on 50 mil centers.

G style FLAT-PAK® • 0.1 grams





Gold plated Kovar® leads are 12 x 4 mils on 50 mil centers.
Base of package is ceramic. Lid is gold plated Kovar®.

Further information

Selling policy: catalog 91-000

Prices: section 91-120

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PRINTED IN U.S.A.

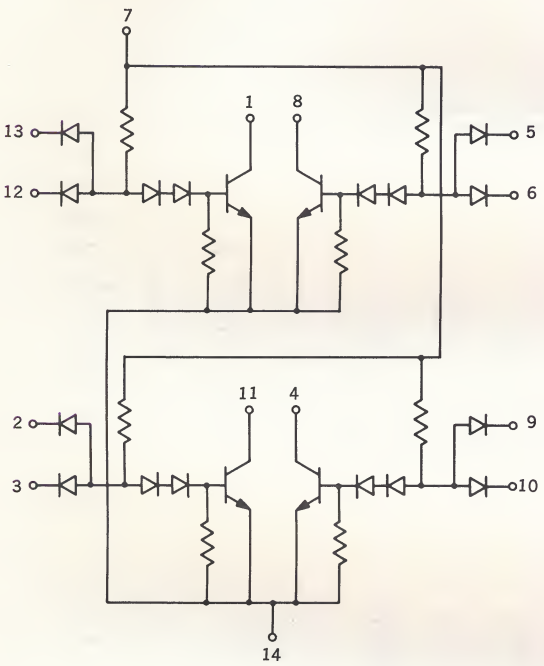
integrated circuits

Quadruple DTL NAND gates

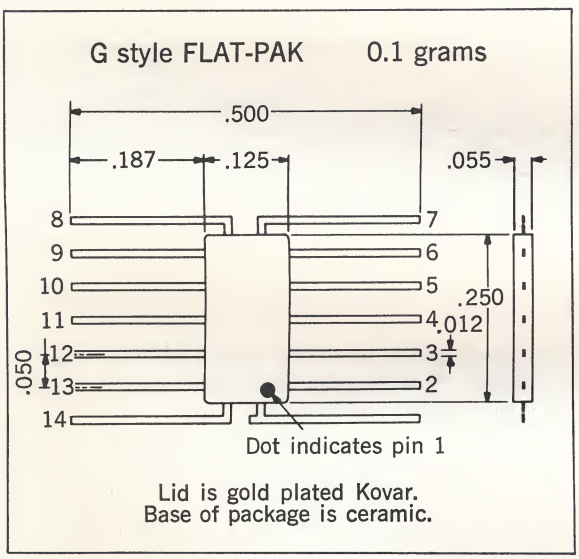
technical data 91-201

WM 246G

Equivalent circuit



Package



Gold plated Kovar® leads are 12 x 4 mils on 50 mil centers. Base of package is ceramic. Lid is gold plated Kovar.

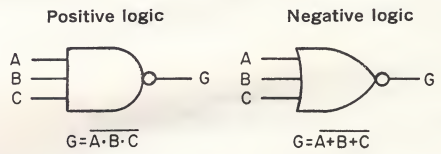
General description

The Westinghouse quadruple DTL NAND gates incorporate four independent gates each having fan-in capabilities of 2. These devices are available in the 14 pin ¼ x ⅛ flat package as shown below. The collectors of these four NAND gates may be externally connected to form an AND-OR-NOT function. Electrical equivalent circuits describing these dual NAND gates are shown on the following pages.

The WM 246G is compatible with all other members of the Westinghouse Molecular DTL logic family.

NAND/NOR function

This gate accomplishes the NAND logic function when the positive logic definition is used. When negative logic is used, the gate accomplishes the NOR logic function. Positive logic results when the more positive of the two voltage levels is defined as the 1-state.



Design features①

- Fan-out 11 minimum
- Noise margin 550 mv minimum
- Switching time 32 ns maximum
- Power consumption 9.5 mw maximum per gate

Reliability assurance

EVERY unit receives

- High temperature storage bake at +150°C
- 3 cycles of thermal shock —55°C to +150°C
- 20,000 G centrifuge
- Gross and helium hermeticity tests

① at V_{cc} = 6.0v and at 25°C

Electrical Characteristics

Absolute maximum ratings①

Parameter	Symbol	Value	Units
Supply voltage	V_{cc}	+10	volts
Input voltage	V_{in}	+10②	volts
Output voltage	V_{out}	+7②	volts
Ambient storage temperature	T_{stg}	−65 to +175	°C
Ambient operating temperature	T_{opg}	−55 to +125	°C

Parameter	Symbol	Limit	Values at temperature			Units
			−55°C	+25°C	+125°C	
Static Electrical Characteristics for $V_{cc} = +6.0$ volts						
Total power consumption, 50% duty cycle	P_c	max.	42	38	30	mw
per package		typ.		30		mw
Input current, input grounded	I_{in}	max.	2.10	1.80	1.50	ma
Input voltage for 0-state output, fan-out of six	$V_{in}/0$	min.	2.30	2.00	1.70	volts
Input voltage for 1-state output, fan-out of one	$V_{in}/1$	max.	1.40	1.00	0.60	volts
Input diode reverse current at $V_{in} = +6.0$ volts	I_R	max.			25	μa
		typ.		0.01	1.0	μa
Output current at the specified $V_{CE(SAT)}$	I_{out}	min.	13.0	20.0	9.0	ma
		typ.		32.0		ma
	$V_{CE(SAT)}$	max.	0.55	0.45	0.35	volts
Output cutoff current for $V_{CEX} = +6.0$ volts	I_{CEX}	max.			30.0	μa
$V_{in} = +0.4$ volts		typ.		0.05	2.0	μa
Fan-out available each gate	F_o	min.	6	11	6	....
Noise margin, worst case③	ΔV_n	min.	0.85	0.55	0.25	volts
Dynamic Electrical Characteristics for $V_{cc} = +6.0$ volts						
Switching time (see figures 1 and 2)						
Turn-on time	T_{on}	typ.	20	24	32	ns
Turn-on time	T_{off}	typ.	22	22	24	ns
Average switching time $(T_{on} + T_{off}) \div 2$	T_{avs}	typ.	21	23	28	ns
		max.		32		ns
Ring propagation delay time, see figure 11) (ring of five gates)	T_{rpd}	typ.	30	30	30	ns

① Limiting values beyond which the serviceability of the device may be impaired.
② These terminals must not be biased negatively with respect to ground.
③ Minimum noise margin is given by: $V_{in}/1 - V_{CE(SAT)}$, where $V_{in}/1$ is the maximum input voltage for a 1-state output, and $V_{CE(SAT)}$ is the maximum output voltage in the 0-state at rated fan-out (6 or 11).

Switching time test circuit and waveforms

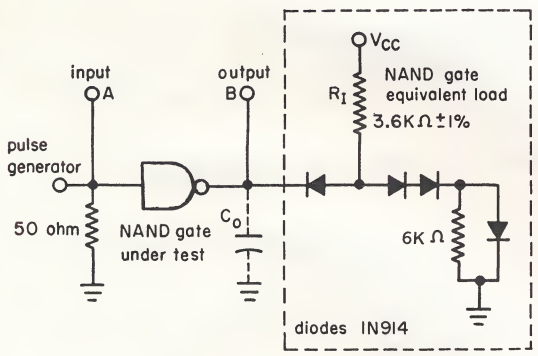


Figure 1 Total capacitance C_o is 10 pf which includes test jig and scope probe. Unused inputs are open circuited.

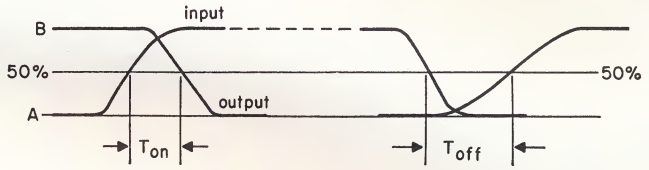


Figure 2 Average switching time: $T_{avs} = \frac{T_{on} + T_{off}}{2}$

Input pulse is 15 ns rise and fall, 200 ns width, 2 volt amplitude, and 100 kc repetition rate.

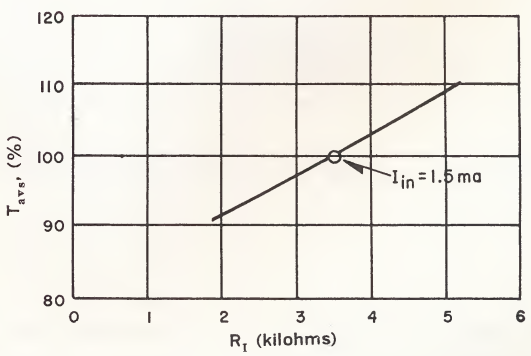


Figure 3 Change in T_{avs} vs. input resistor value R_I at 25°C.

Typical electrical characteristics

Output and input current vs. temperature and supply voltage

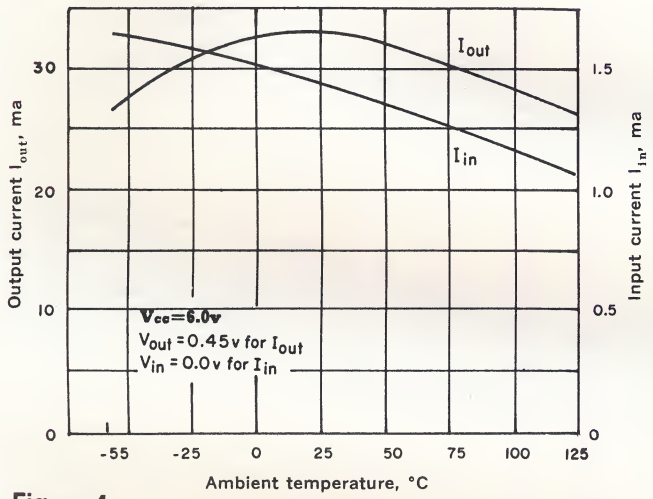


Figure 4

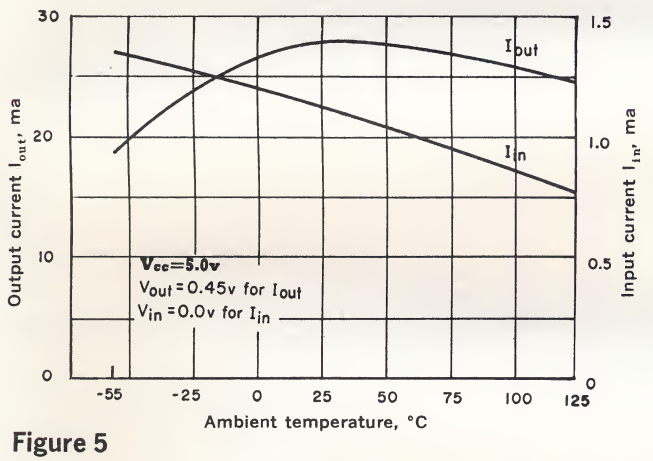


Figure 5

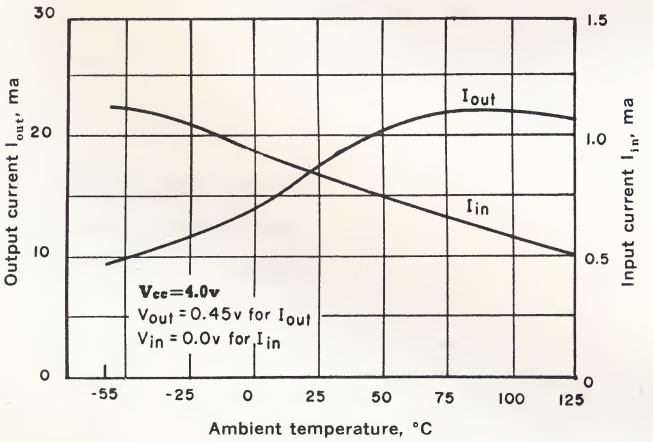


Figure 6

Output saturation characteristic vs. temperature

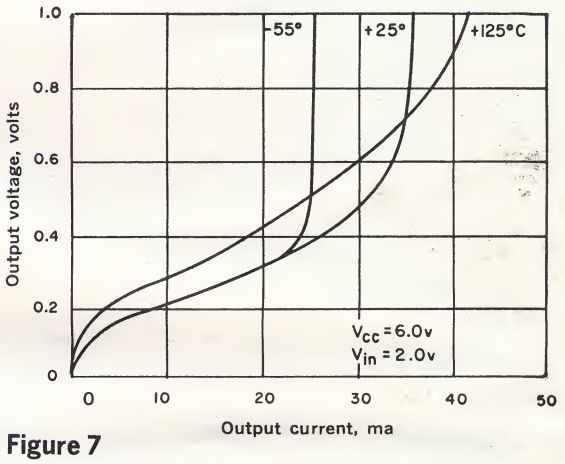


Figure 7

Output voltage vs. input voltage and temperature

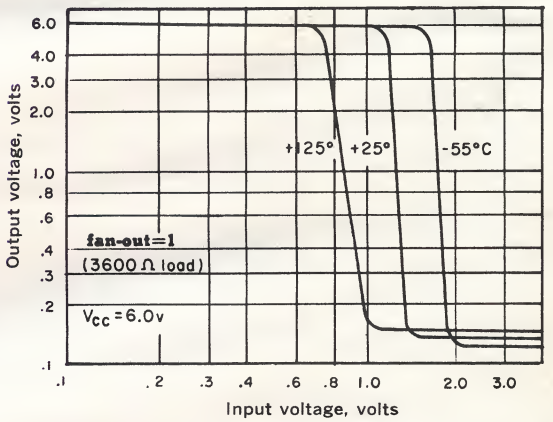


Figure 8

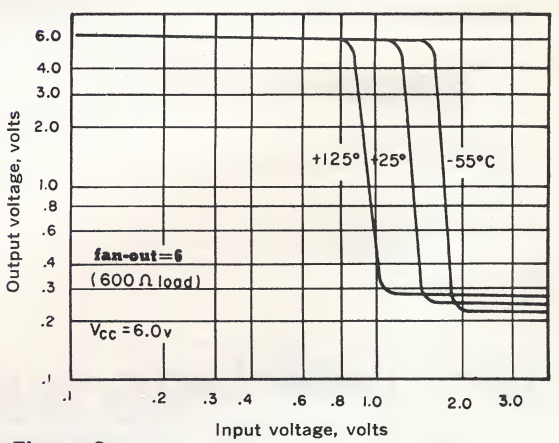


Figure 9

Typical electrical characteristics

Power consumption (50% duty cycle).

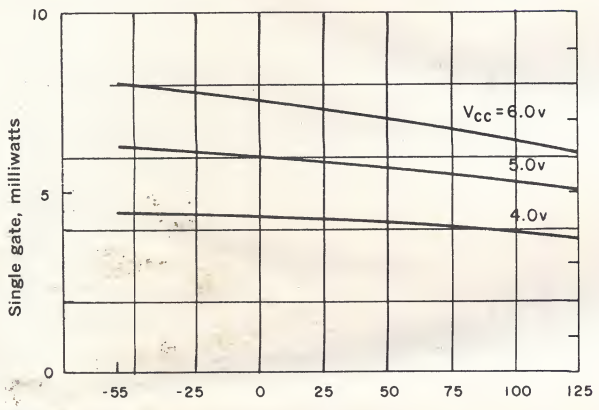


Figure 10

Ring propagation delay time vs. supply voltage and temperature

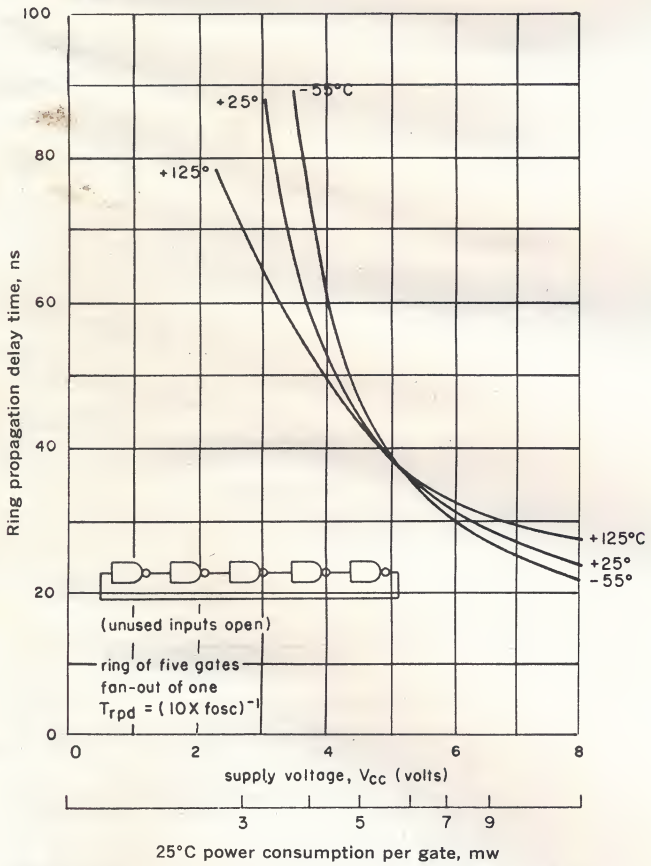


Figure 11

Fan-out test circuit (all integrated gates)

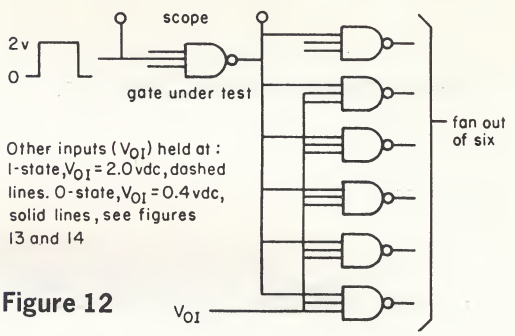


Figure 12

Propagation time vs. fan-out

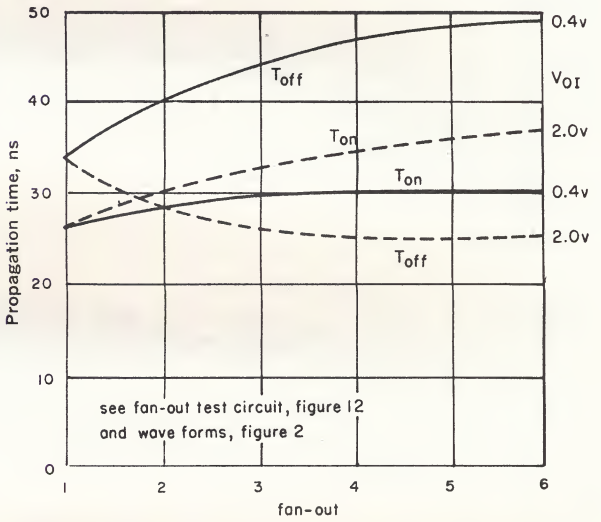


Figure 13

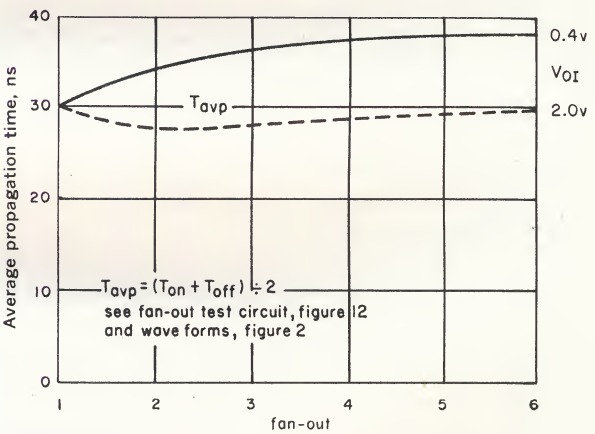


Figure 14

Further information

Selling policy: catalog 91-000

Prices: section 91-120

Westinghouse Electric Corporation / *MOLECULAR ELECTRONICS DIVISION*

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integrated
MOLECULAR
circuits

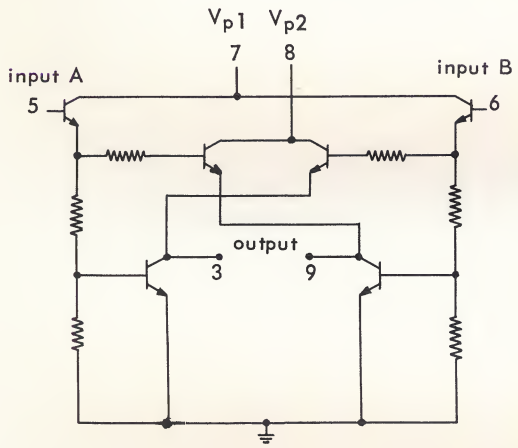
destructive readout bit driver

technical data 91-181

WS 151Q

page 1

silicon planar epitaxial monolithic
integrated electronic blocks
for digital systems



general description

The Westinghouse WS 151Q is a planar epitaxial silicon integrated circuit providing the function of a destruct readout core driver which may be utilized in driving memory core with currents up to 150 ma.

design features

- high input impedance, low driving impedance
- low power dissipation
- one power supply capability
- high speed
- output current greater than 100 ma.

reliability assurance

EVERY unit receives

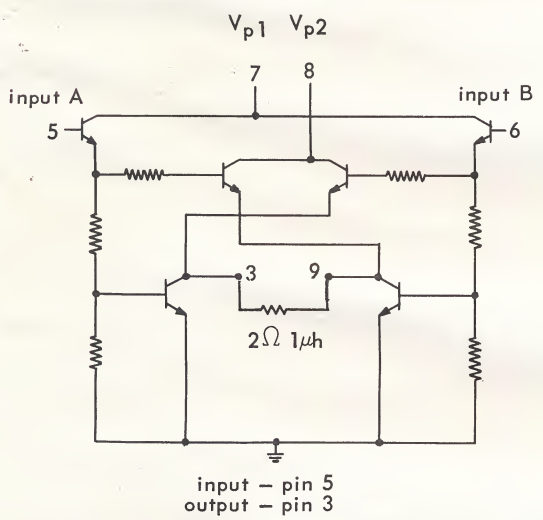
- high temperature storage bake at +150°C
- 3 cycles of thermal shock —55°C to +150°C
- 20,000 G centrifuge
- gross and helium hermeticity tests

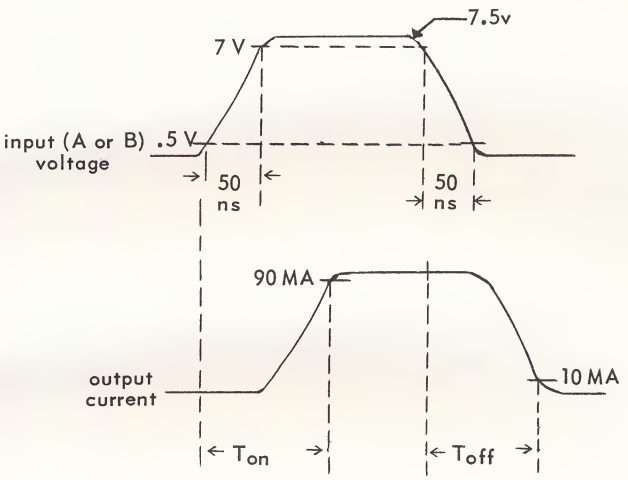
parameter	value	units
absolute maximum ratings①		
supply voltage	15	volts
input voltage	9	volts
output voltage	10	volts
ambient storage temp.	—65 to +175	°C
ambient operating temp.	— 0 to +125	°C

① Limiting values beyond which the serviceability of the device may be impaired.

Parameter (V_{p1} = V_{p2} = 10v)	Condition	Symbol	Limit	Value	Units
static electrical characteristics (25°C)					
Input Impedance		Z_{in}	Min.	5	kohms
Input Voltage	I_{out}= 130ma	V_{in}	Max.	7.5	volts
Output Saturation Voltage	I_{out}= 100ma	$V_{CE(SAT)}$	Max.	1	volts
Power Consumption	25% duty cycle	P_c	Max.	150	mw
Input Current	V_{in}= 7.5v	I_{in}	Max.	1.5	ma
dynamic electrical characteristics					
Turn on time		T_{on}	Max.	100	ns
Turn off time		T_{off}	Max.	350	ns

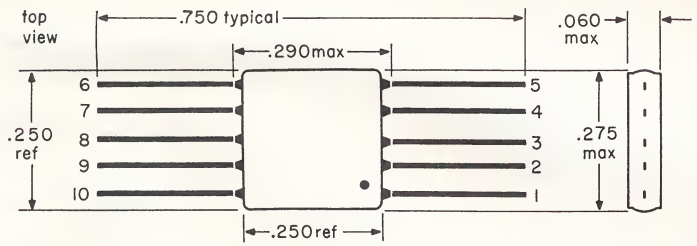
switching time test circuit and waveforms





mechanical characteristics

Q style FLAT-PAK 0.25 grams



Gold plated Kovar ® leads are 15 x 5 mils on 50 mil centers.

pin connections

1	Ground	6	Input B
2	no connection	7	Supply
3	Output A	8	Supply
4	no connection	9	Output B
5	Input A	10	no connection

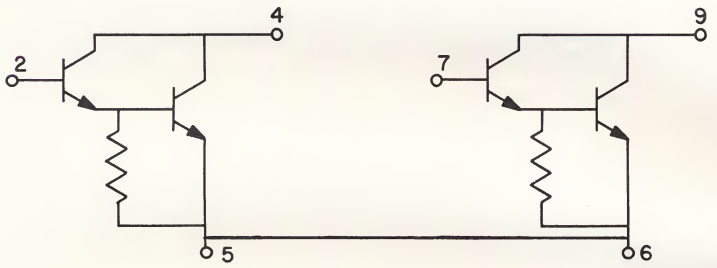
further information

condensed catalog 91-000

prices: section 91-120

silicon planar epitaxial monolithic
integrated electronic blocks
for analog systems

circuit schematic



design features

- *high package density*
- *high beta*
- *high input impedance*
- *low* V_{sat}

reliability assurance

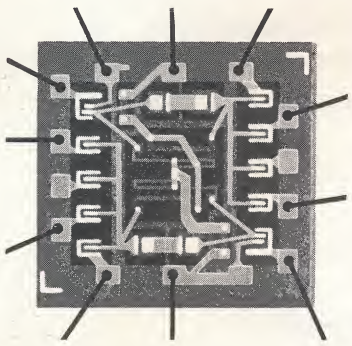
EVERY unit receives

- high temperature storage bake at +150°C
- 3 cycles of thermal shock −55°C to +150°C
- 20,000 G centrifuge
- gross and helium hermeticity tests

general description

The WS 153Q high current dual darlington is a silicon planar epitaxial monolithic integrated circuit consisting of two isolated medium power darlington switches. It is useful at current levels up to five hundred milliamperes and voltage levels up to twenty-five volts.

electrical characteristics



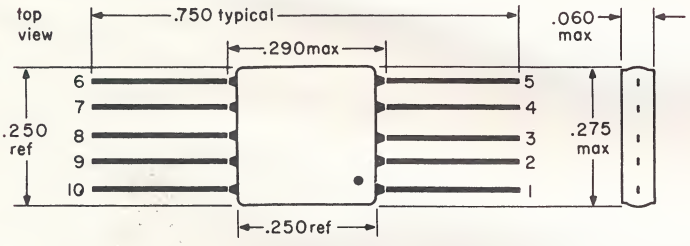
typical planar
epitaxial silicon
integrated circuit

parameter	value	units
absolute maximum ratings①		
BV_{EBO}	7	volts
LV_{CEO}	20	volts
BV_{CBO}	40	volts
ambient storage temperature		−65° C to +175° C
ambient operating temperature		−55° C to +125° C

Parameter	Condition	Value	Limit	Units
static electrical characteristics at 25°C				
h_{fe}	I_c =100 ma	500	min.	
$V_{CE(SAT)}$	I_c =500 ma I_b=10 ma	1.5	max.	volts
I_{CBO}	V_{CB}=20v	5	max.	μa
I_{EBO}	V_{EB}= 5v	5	max.	μa
dynamic electrical characteristics at 25°C				
$T_R + T_D$	I_c = 100 ma	150	typ.	ns
$T_F + T_S$	I_b = 1 ma	150	typ.	ns

mechanical characteristics

Q style FLAT-PAK • 0.25 grams



Gold plated Kovar® leads are 15 x 5 mils on 50 mil centers.

pin connections

1	No connection
2	Input A
3	No connection
4	Output A
5	Ground
6	Ground
7	Input B
8	No connection
9	Output B
10	No connection

further information

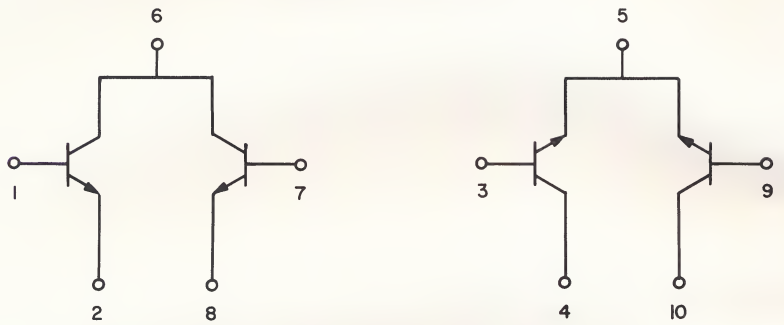
condensed catalog 91-000

prices: section 91-120

① Limiting values beyond which the serviceability of the device may be impaired.

silicon planar epitaxial monolithic
integrated electronic blocks.

circuit schematic



design features

- *high breakdown voltage*
- *F_T over 200 megacycles*
- *I_c greater than 1 amp*
- *low saturation voltage V_{ce} (Sat)*
- *multiple core driving capability*
- *isolated pairs*

reliability assurance

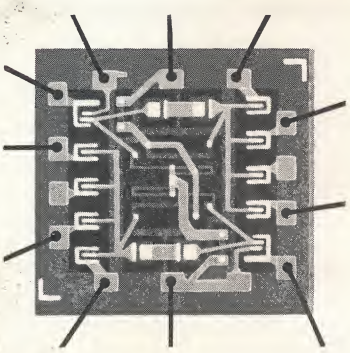
EVERY unit receives

- high temperature storage bake at +150°C
- 3 cycles of thermal shock −55°C to +150°C
- 20,000 G centrifuge
- gross and helium hermeticity tests

general description

The WS 154Q is a silicon planar epitaxial integrated circuit consisting of four high speed medium power isolated transistors mounted in one package. The transistors are suitable for operation at current levels up to one ampere and voltage levels up to twenty-five volts. The transistors may be connected in other specified circuit configurations to offer a multiplicity of functional variations.

electrical characteristics



typical planar, epitaxial silicon integrated circuit

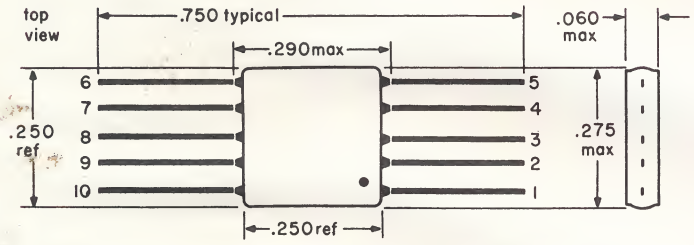
absolute maximum ratings①

ambient operating temperature	—0°C to +125°C
ambient storage temperature	—65°C to +175°C
average power per package	+.5 watts

parameter	conditions	value	limit	units
static electrical characteristics @ 25° C				
I_{CBO}	$V_{CB} = 30V$	1	max.	μa
I_{EBO}	$V_{EB} = 5V$	10	max.	μa
V_{CEO}	*I_{CE} = 100ma	30	min.	volts
h_{fe}	I_c = 100ma V_c = 1.0V	30	min.	—
h_{fe}	*I_c = 1 amp V_C = 2.0V	15	min.	—
$V_{CE(SAT)}$	*I_c = 1.0 amp I_B = 100ma	1	max.	volts
C_{OB}	$V_{CB} = 10V$	15	max.	pf
f_t	$V_{CE} = 10V$	200	typ.	mc
LV_{CEO}	—	30	—	volts
BV_{CBO}	—	60	—	volts
BV_{EBO}	—	7	—	volts

* Test made with 300 μsec., 2% duty cycle pulse.

Q style FLAT-PAK • 0.25 grams



Gold plated Kovar® leads are 15 x 5 mils on 50 mil centers.

pin connections

1	Base A
2	Emitter A
3	Base C
4	Collector C
5	Emitter C & D
6	Collector A & B
7	Base B
8	Emitter B
9	Base D
10	Collector D

① Limiting values beyond which the serviceability of the device may be impaired.

further information

condensed catalog 91-000

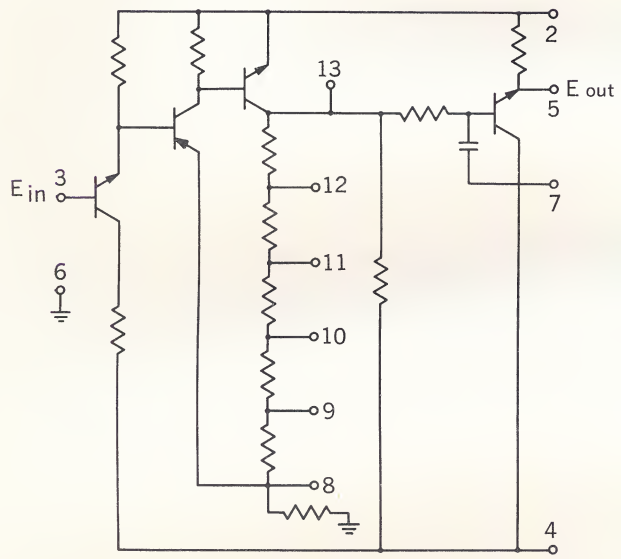
prices: section 91-120

integrated circuits

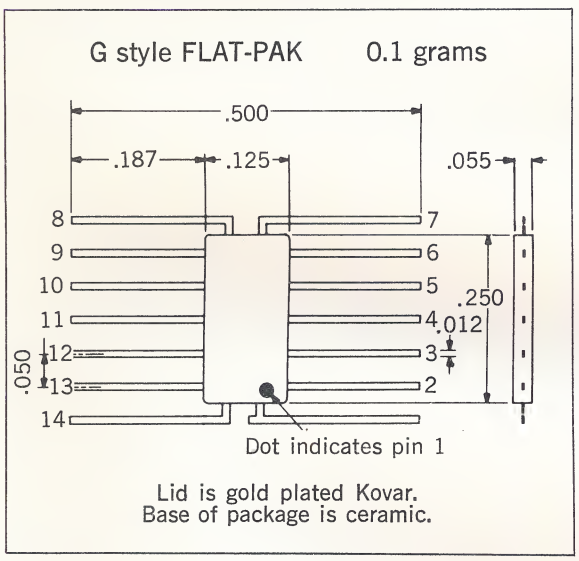
read preamplifier
technical data 91-191

WS 934

Equivalent circuit



Package



Description and application

The Westinghouse WS 934 is a four-stage voltage amplifier with external taps for controlling the gain. It is designed as a magnetic pick-up read preamplifier capable of compensating for head-to-head signal level variations. It is particularly well suited to computer readout from drum, disc or tape memories.

It also performs well as a general purpose voltage amplifier with an output capability greater than one volt rms and a frequency response beyond one megacycle. A capacitor is included to roll-off the gain above 900 kc if desired.

The WS 934 is a monolithic silicon block. It contains both pnp and npn transistors and is fabricated by planar epitaxial techniques. It is packaged in a Westinghouse standard glass Kovar® FLAT-PAK™ with a ceramic base and gold plated leads. Dimensions are ¼" x ⅛" exclusive of leads and weight is approximately 0.1 gram.

Design features

- High input impedance (180 KΩ)
- Low output impedance (100Ω)
- Frequency response to 1 mc
- Gain of 30 at mid-frequency
- Gain variable in 32 increments

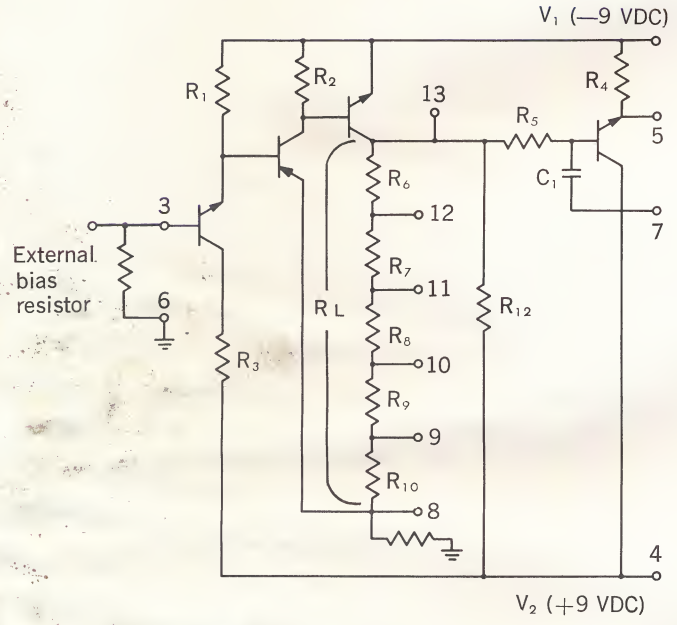
Reliability assurance

EVERY unit receives

- 150°C bake for 24 hours minimum
- 3 cycles of thermal shock
  −55°C to +150°C
- 20,000 G centrifuge
- Gross and helium hermeticity tests

WS 934 read preamplifier

technical data 91-191



Nominal circuit parameters

C_1	68 uufd	R_4	10 K	R_8	4 K	R_{12}	8 K
R_1	36 K	R_5	3 K	R_9	2 K	R_L	0-31K
R_2	4 K	R_6	16 K	R_{10}	1 K		
R_3	5 K	R_7	8 K	R_{11}	1 K		

Absolute maximum limits

Power dissipation	200 milliwatts
Input breakdown voltage	9 volts
Supply voltages	±10 volts
Input voltage: Non-operating	±10 volts
Power application sequence	(no restriction)
Storage temperature range	—65 to +175°C

Test conditions

Circuit as shown above
Input bias resistor = 20 KΩ
V_{CC} = 9 volts
Temperature range 0-60°C
C_1 grounded

Electrical characteristics

Characteristic	Conditions	Symbols	Values Min	Values Typical*	Values Max	Units
Current drain	Pin 3 grounded	I_1	—	2.3	3.5	milliamperes
		I_2	—	2.3	4.5	milliamperes
AC input impedance	Pins 8 through 13 open E_{in} = 100 mv p-p @160 kc	Z_{in}	18 (1)	19.5	20	kilohms
AC output impedance		Z_{out}		100	250	ohms
Off-set voltage	Bias resistor = 4.7 KΩ Pin 3 grounded	△V △V	—3 —3		+3 +3	volts volts
AC voltage gain at 160 kc (2)	Pin 13 connected to 11 Pin 10 connected to 8	V_4	4.4	5.2	5.9	volts/volt
	Pin 13 connected to 12 Pin 11 connected to 9	V_9	8.8	9.7	10.6	volts/volt
	Pin 12 connected to 8	V_{16}	14.7	16.7	17.7	volts/volt
	Pins 8 through 13 open	V_{31}	25.8	30.0	32.5	volts/volt
AC voltage gain at 320 kc	Pins 8 through 13 open	V_{31}	23.4		31.5	volts/volt
Phase shift at 320 kc (3)	Pins 8 through 13 open	0	0.2	0.25	0.5	microsecond

* Based on measurements taken on 700 devices.

Note 1: This is input impedance of the device with the 20 KΩ input bias resistor. An impedance of greater than 180 KΩ looking into device terminals 3 and 6 is thus insured.

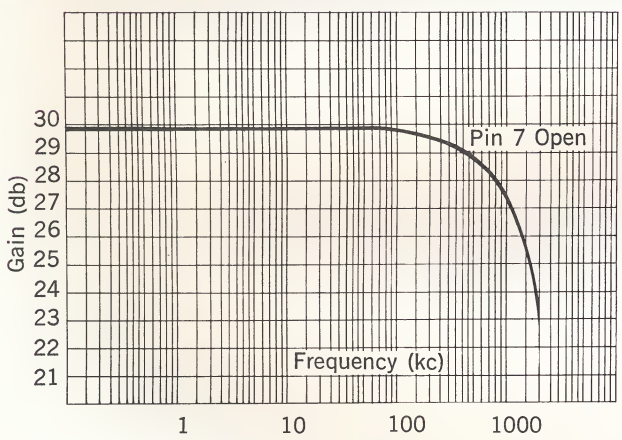
2: Connections for four gain steps are measured on all devices. These connections assure all load resistor segments and taps in the spec. Input voltage 100 mv p-p.

3: Measured from displacement of axis crossing of input and output waveforms.

Connections for gain increments

LOAD RESISTOR TAP CONNECTIONS			EFFECTIVE LOAD RESISTOR (R_L)	NOMINAL GAIN (volts/volt)
Pin to Pin	Pin to Pin	Pin to Pin		
13 to 9			1 K ohms	2.25
13 to 10	9 to 8		2 K	3.2
13 to 10			3 K	4.0
13 to 11	10 to 8		4 K	5.2
13 to 11	10 to 9		5 K	5.8
13 to 11	9 to 8		6 K	6.7
13 to 11			7 K	7.6
13 to 12	11 to 8		8 K	8.6
13 to 12	11 to 9		9 K	9.7
13 to 12	11 to 10	9 to 8	10 K	10.7
13 to 12	11 to 10		11 K	11.6
13 to 12	10 to 8		12 K	12.6
13 to 12	10 to 9		13 K	13.6
13 to 12	9 to 8		14 K	14.6
13 to 12			15 K	15.6
12 to 8			16 K	16.7
12 to 9			17 K	17.7
12 to 10	9 to 8		18 K	18.7
12 to 10			19 K	19.7
12 to 11	10 to 8		20 K	20.7
12 to 11	10 to 9		21 K	21.7
12 to 11	9 to 8		22 K	22.7
12 to 11			23 K	23.7
11 to 8			24 K	24.7
11 to 9			25 K	25.7
11 to 10	9 to 8		26 K	26.6
11 to 10			27 K	27.4
10 to 8			28 K	28.2
10 to 9			29 K	28.8
9 to 8			30 K	29.3
None			31 K	30.0

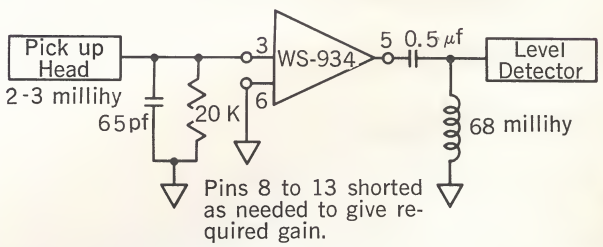
Gain vs. frequency for WS 934



Typical applications

- Read preamplifier for computer magnetic disc memory
- Buffer or compensating amplifier

Read Preamplifier – computer magnetic disc memory: bit rate of 320 KC



View showing the extensive cleanroom facilities in continuous operation for the manufacture of Westinghouse Integrated Circuits.

Westinghouse Electric Corporation / *MOLECULAR ELECTRONICS DIVISION*

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OEM PRICE LIST

COMMERCIAL DTL (0°C to +75°C)

type number and description			net unit price quantity 50-499	1-49
	WC 204G	Single NAND Gate, Four Input with Node	$ 5.00	$ 6.80
	WC 204T	Single NAND Gate, Four Input with Node	6.20	8.50
	WC 214G	Single NAND Gate, Six Input with Node	5.00	6.80
	WC 214T	Single NAND Gate, Six Input with Node	6.20	8.50
*	WC 224G	Single NAND Gate, Eight Input with Nodes	5.00	6.80
	WC 224T	Single NAND Gate, Eight Input with Nodes	6.20	8.50
	WC 201G	Dual NAND Gate, Three Input	5.70	7.80
	WC 201T	Dual NAND Gate, Three Input	7.10	9.70
	WC 211G	Dual NAND Gate, Four Input	6.00	8.20
	WC 211T	Dual NAND Gate, Four Input	7.50	10.50
	WC 221G	Dual NAND Gate, Three Input with Node	6.00	8.20
	WC 221T	Dual NAND Gate, Three Input with Node	7.50	10.50
*	WC 231G	Dual NAND Gate, Four Input with Node	6.00	8.20
	WC 241G	Dual NAND Gate, WC 211G with Collector Resistors	6.00	8.20
*	WC 261G	Dual NAND Gate, WC 231G with Collector Resistors	6.00	8.20
	WC 206G	Triple NAND Gate, 2 Three Inputs, 1 Two Input with Node	7.10	9.70
*	WC 216G	Triple NAND Gate, 3 Three Inputs	7.10	9.70
	WC 226G	Triple NAND Gate, WC 206 with Collector Resistors	7.10	9.70
*	WC 236G	Triple NAND Gate, WC 216 with Collector Resistors	7.10	9.70
*	WC 246G	Quad NAND Gate, 4 Two Input	7.80	10.50
*	WC 266G	Quad NAND Gate, WC 246 with Collector Resistors	7.80	10.50
*	WC 286G	Hex NAND Gate, 6 One Input	9.55	13.10
*	WC 296G	Hex NAND Gate, WC 286 with Collector Resistors	9.55	13.10
	WC 202G	RS Flip-Flop, Three Input	6.60	9.00
	WC 202T	RS Flip-Flop, Three Input	7.80	10.50
*	WC 212G	RS Flip-Flop, Three Input with Node	6.90	9.40
	WC 212T	RS Flip-Flop, Three Input with Node	8.60	11.70
*	WC 213G	Pulse Binary Counter	7.60	10.40
	WC 213T	Pulse Binary Counter	9.50	12.70
*	WC 215G	JK Flip-Flop	7.60	10.40
	WC 215T	JK Flip-Flop	9.50	12.70
	WC 217G	Diode Expander, Seven Input	3.70	5.10
	WC 217T	Diode Expander, Seven Input	4.60	6.40
*	WC 227G	Diode Expander, Ten Input	4.10	5.60
*	WC 210G	Line Driver, 2 Three Input	7.20	9.80
	WC 210T	Line Driver, 2 Three Input	9.50	12.70
*	WC 208G	Level Detector — Schmitt Trigger	9.50	12.70
	WC 208T	Level Detector — Schmitt Trigger	12.50	17.10

June 1, 1965

Prices effective June 1, 1965, subject to change without notice

Supersedes Issue of February 21, 1965

For Standard terms and conditions of sale, refer to Selling Policy 91-000

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